Noah Zhang

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Education

University of Illinois Urbana-Champaign **Aug 2023 - May 2027**

Bachelor of Science in Computer Engineering *GPA: 3.7/4.0*

Illini Solar Car, Divergence 2% AI Lab | Specialized Courses: Computer Systems, RTL Design, Digital Systems Laboratory

Experience

Astiva Health **Oct. 2025 – Present**

Software Engineering Intern *Remote*

- Developing ICD-10 code identification pipeline for processing medical records with Python OCR and LLM reasoning.
- Handwritten OCR training and finetuning with TrOCR, Azure Document Intelligence, and text embedding model.
- Integrating pipeline with company's existing SQL server for ICD-10 code storage, auditing, and patient analytics.
- Building a secure full-stack review interface in React/Python for medical record visualization and code verification.

Cognition AI **May 2024 – Aug. 2024**

Development Intern *Remote*

- Researched and wrote playbooks for Devin's common dev tasks: web deployment, unit tests, API integration, front-end.
- Triaged and bug-hunted customer runs to generate training samples for Devin.
- Cloned Devin instances (improving speed and reliability) to parallelize rewriting all unit tests in MetaMask's repository.

Astiva Health **Feb 2024 – May 2024**

Software Engineering Contractor *Los Angeles, CA*

- Developed automated CMS 1500 claims filing application adhering to HL7 and HIPAA data standards.
- Trained object recognition model using Python and OpenCV to analyze handwritten claim documents.
- Built a QA workstation in Python Tkinter for reviewing automated claims processing.

Quartic Solutions **Jun 2022 – Aug 2022**

Software Engineering Intern *San Diego, CA*

- Automated internal employee bandwidth monitoring and customer profiles in Smartsheet and Python.
- Reorganized existing company internal tracking to efficiently scale with new hires and new customers.

Leonardo DRS **Sep 2021 – Dec 2021**

Engineering Intern *San Diego, CA*

- Engineered a MIL-SPEC testing environment for Quadrax–Octonet fiber links in missile detection systems.
- Designed RTL modules in SystemVerilog to simulate 8b/10b encoded high-speed data transfer.
- Deployed and verified FPGA prototypes ensuring signal integrity and protocol compliance.
- Assigned project lead for five other interns and attained record progress on project completion.

Projects

RISC-V Operating System | *C, RISC-V Assembly, QEMU, Linux*

- Developed an OS kernel for RISC-V architecture including memory management, file system, and interrupts.
- Implemented console I/O, device driver interface, and exception/interrupt service routines in C and assembly.
- Implemented virtual memory with page tables, address translation, and dynamic memory allocation.

FPGA OSU! Rythm Game | *C, SystemVerilog, Vivado, Vitis, FPGA*

- Built a rhythm game on FPGA using HDMI video output and AXI peripherals driven by a MicroBlaze soft-core.
- Built a VRAM implementation with hardware acceleration for displaying game objects and glyphs.
- Implemented game logic, hit detection, and timing modules in SystemVerilog/C; integrated using Vivado IP cores.

Endless Wordhunt | *JavaScript, Firebase, Tailwind, HTML, CSS*

- Built an online 4x4 word game with over 2,000 unique monthly players
- Developed a real-time 4×4 word-search engine with DFS + prefix-set pruning, finding all legal words in <5ms

Technical Skills

Languages: C/C++, C#, Python, SystemVerilog, SQL, RISC-V Assembly, JavaScript, HTML/CSS
Developer Tools: Git, Vivado, Vitis, Linux, Torch, Docker, Firebase, SSMS, Azure, OpenCV, Tesseract OCR